SEL\_RNG: 1 means external RNG input is used.

SEL\_DIRECT: Control topology of RNG generation block. You can try both to see which gives more randomness.

SEL\_CLK\_SLOW, SEL\_CLK\_FAST: 1 means internal VCO clock is chosen, else, external clock is chosen for the clocks for RNG

SEL\_CLK: 1 means external system clock is chosen

SEL0\_WR, SEL1\_WR: Sets pulse widths for write for memory timing block. 01 works in sim. You can try others depending on chip corner.

SEL1\_RD, SEL0\_RD : Sets pulse widths for read for memory timing block. 01 works in sim. You can try others depending on chip corner.

FAST: If clock period is lower than 2us, use fast = 0. Memory speed is limited by write. It can’t be lower than 1.5us

DATA\_FROM\_EXT: Keep this 1 while writing to the memory. Else 0.

CTRL\_MEM\_SOURCE: Keep this 1 while writing to the memory. Else 0.

CTRL\_DATA\_SOURCE: Keep this 0 to bypass the memory, and use the external data to directly feed the encryption block

BRDN2, BRDN1, BRDN0: Set the strength of the SA in memory. 001 works in sim. You can try others depending on chip corner.